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Level set based topology optimization of directly bonded copper substrates targeting thermal stress minimization on die-substrate bonding line

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1. Abstract

Power module is a key power component in hybrid and electric vehicles. It electrically connects the batteries and driving motors, and provides multiple functions: driving motor power, regenerating power, boosting operational voltage, and charging batteries. Due to these multiple functions, power modules are exposed to high power density and experience high operational temperatures (recently reaching 125-150 °C). Such high temperature imposes significant reliability challenges and often leads to critical damage. In such situations, multi-physics topology optimization is expected to be a key technology to enhance performance [1].

Substrate failure is a typical example of high temperature-induced damage. Direct bond copper (DBC) substrates are popularly used in recent power module designs due to superior thermal performance. A DBC substrate consists of an insulating ceramic layer sandwiched by two copper layers. Often, additional materials may be deposited on top of the copper layers. The two different materials have distinct thermal properties including coefficient of thermal expansion (CTE). Copper has a CTE that is 3-5 times larger than those of ceramic materials used in power module substrates. The CTE mismatch results in significant thermally-induced stress at the interfaces between the power die and substrate, and causes die failure. Therefore, for reliable power modules, it is critical to minimize the thermally-induced stress and suppress the damage in the die and corresponding bonding layer. Various efforts related to fabrication and material design have been devoted to solving such damage problems. Stress reduction may be achieved by varying the thickness of the ceramic or metal layers. However, beyond material change or thickness modification, a new approach related to thermal-stress reduction and delamination prevention is focused on modifying the overall substrate dimensions (e.g. size) and introducing a step layer at the edges of the metal layer [2]. This interesting approach suggests the use of numerical optimization methods in the resolution of thermal-stress and delamination issues in power module substrates.

In this research, level set based topology optimization is applied to the design of the copper layer of the DBC substrate to minimize thermally-induced stress at the bonding layer between the device and metallic layer of the DBC. Here, we adopt a two-dimensional (2-D) pattern design approach instead of a cross-sectional configuration design strategy to avoid additional changes to the fabrication process. First, a 2-D level set field is prepared for the design variables, and then the level set contour is projected into a three-dimensional model for finite element analysis. The optimization code was implemented based on level set topology optimization with a geometric re-initialization scheme [3]. Finally, a 2-D design is directly obtained, which is utilized as a photo mask pattern for fabrication of a prototype DBC.

To date, the optimization code has been implemented, and the effectiveness of the method has been numerically confirmed. Additionally, prototypes have been fabricated using the optimized photo mask pattern. These results are provided in the conference.

2. Keywords: Topology optimization, level set, thermally-induced stress, power module, electric vehicles

3. References

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